IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Patent Application No. 10/541,275

Confirmation No. 6275

Applicant: Moreira et al.

Filed: June 30, 2005

TC/AU: 2183

Examiner: Keith E. Vicary

Docket No.: 260686 (Client Reference No. P81933US00)

Customer No.: 23460

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants request review of the final rejection, dated March 30, 2009, in the above-identified application. No amendments are being filed with this request. This request is being filed with a notice of appeal. An appeal brief has not yet been filed. This Pre-Appeal Brief Request For Review is submitted for the reasons stated on the attached sheets.

Remarks

Appellants traverse the continued rejection of the pending claims. In particular, Appellants traverse the rejection of independent claims 1 and 29 under 35 U.S.C. § 102(b) as being anticipated by Gove et al., U.S. Pat. No. 5,212,777 (Gove). Appellants previously amended claim 1 to recite that processing elements are coupled together using a **reconfigurable channel infrastructure** including: (1) a control chain with combination elements for each processing element and (2) a switch between each pair of neighboring processing elements to controllably inhibit transmission of intermediate control signals (e.g., L1, L2, etc. in Figs. 5 and 6) to a neighboring element. The aforementioned reconfigurable channel arrangement facilitates a "serial" linking of processing elements together without relying on a cross-bar switch structure of the type disclosed on Gove.

In an effort to minimize the issues addressed during this requested review, Appellants focus upon the rejection of independent claim 1 (reciting elements similar to independent claim 29) due to clear errors in the Office Action regarding this claim. Independent claims 1 and 29 are provided in an Appendix attached hereto.

Summary of Claimed Subject Matter

According to the invention recited in independent claim 1, the processing elements are coupled by **a reconfigurable channel infrastructure that includes a control chain with combination elements** (e.g., combination elements "c" in Fig. 5) for each processing element (e.g., processing element PE in Fig. 5) and a switch (e.g., switch SW in Fig. 5) between each pair of neighboring processing elements. The switch controllably inhibits transmission of intermediate control signals (e.g., L1 and L2 in Fig. 5) to a neighboring processing element. Thus, the switches are used to serially pass control signals shared by a cluster of processing elements.

The recited invention facilitates providing a dynamically reconfigurable parallel processor at any scale. For example, the processing apparatus as shown in FIG. 5, for which two processing elements are shown, can be extended to multiple times more units by extending the control chain (CHN). The same extension of processing system is enabled by extending the control chain disclosed, by way of both general and specific examples, in the written description.

Thus, in the recited invention, a plurality of processing elements can be dynamically configured via the control chain (CHN) to operate under a common thread of control. In the claimed dynamically reconfigurable multiprocessor arrangement, a cluster of processing elements is defined by cluster boundaries. For example, in Figure 5, by configuring a first switch before a processing element PE_n, and a second switch after a processing element PE_m coupled to the control chain as non-transmitting, any intermediate cluster control signal will not be exchanged/passed by these two switches to the defined chain. Thus, the set of processing elements N, N+1, N+2, ..., M-1, M forms a cluster that operates independently from the processing elements beyond the switches that are coupled to either end of the configured processing element cluster.

Gove's Disclosed Multiprocessor System

Gove discloses a multiprocessor system that includes a single bus structure connecting a set of processing elements. Gove's disclosed multiprocessor includes four primary components: (1) processors, (2) a cross-bar switch 20, (3) memory cells containing instructions and data, and (4) **a synchronization control bus 40 that carries control signals for programming and executing the synchronization statuses of the processors**. *See*, Gove, FIGs. 1, 4 and 22.

Gove utilizes a universal bus hardware arrangement to control sharing of data/control between processors. In particular, each processor includes a synch control register indicating the processors with which the processor should be synchronized (for data and/or instructions), and each processor has, for each of the other processors, a respective NAND gate connected to the respective signal line and the respective bit for the other processors. In the Gove arrangement where each processor-to-processor element communication path is direct, the number of control bus lines 40 increases linearly with the increase in the number of processing elements. Moreover, the number of configuration bits increases with the *square* of the number of processing elements.

Thus, in summary, Gove's cross-bar switch connects categorized (grouped) processors with the appropriate memory cells. *See*, Gove, col. 2 lines 47-53. As shown in FIGs. 4 and 22, Gove provides a continuous set of synchronization control signal lines 40 to which synchronization control logic for *each* processing element is connected *in parallel*.

Gove's Processor Architecture Disclosure Does Not Anticipate Appellants' Claims

Gove does not disclose Appellants' claimed multiprocessor system recited in claim 1. The claimed invention includes a reconfigurable channel infrastructure comprising a *control chain* which cannot be found anywhere in Gove. Furthermore, claim 1 recites the control chain includes a *switch between neighboring processors that locally controllably inhibits transmission of intermediate control signals to a preceding or succeeding processing element in the control chain.* In contrast to the express language of claim 1, in the multi-processor synchronization control scheme depicted in FIG. 22 of Gove, the NAND gates associated with particular ones of the processing elements cannot **controllably inhibit transmission of the synch control signals on synchronization lines 40 to neighboring processing elements.**

Gove's universal control bus architecture is the antithesis of Appellants' claimed invention. Gove's "cross-bar switch" based cluster control architecture includes a universal bus and a set of individual direct-connect logic circuits to match processors with instructions located in memory to achieve clustering. In contrast, Appellants' claimed invention includes a reconfigurable channel infrastructure comprising a *control chain* (communicatively connected to the 2D grid of processing elements as shown in Appellants' FIG. 7) that sends controls signals *serially* via intermediate paths *between serially connected links to the processing elements* to achieve clustering.

Moreover, Gove's configurable cluster control logic/circuitry does not include *switches* inserted between, and controlling passage of intermediate cluster control signals between neighboring processing elements. The recited switches, interposed on the control chain between neighboring processing elements, serve the essential functionality of determining when to transmit intermediate control signals to processing elements attached to the control chain.

In summary, Gove implements multiprocessor cluster control in a way that substantially/literally differs from the recited cluster control hardware recited in claim 1. Gove discloses universal bus-based cluster control logic. Nowhere does Gove disclose or even remotely suggest Appellants' recited control chain including a set of switches implementing localized serial cluster control of a set of processing elements. **Gove achieves clustering via a cross-bar switch wherein each processor is provided with individual direct connections to a universal set of cluster control signal lines.** Meanwhile, Appellants' claimed reconfigurable

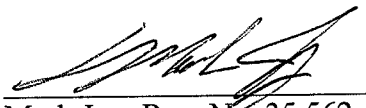
channel infrastructure includes a *control chain* for passing cluster signals to the processing elements via switches capable of locally inhibiting transmission of intermediate cluster control signals to neighboring links of the control chain.

Claim 29 is similarly distinguishable from Gove's disclosed cluster control hardware. Claim 29 recites "combining" and "deriving" steps including limitations directed to control chain-based (including using *two or more intermediate control signals*) propagation of cluster control signals for a set of processing elements through the use of intermediate control signals. Gove does not disclose at least the recited intermediate control signals to derive a cluster control signal for processing system including a plurality of processing elements.

Conclusion

For the reasons stated herein above, the presently pending claims are patentable over the prior art presently known to Appellants. The final rejection of the presently pending claims is based solely upon an unsupportable broad interpretation of certain identified elements of Appellants' claims. Appellants therefore request early (pre-appeal brief) review (and reversal) of the final rejection of the presently pending claims 1-6, 8-14, and 16-29.

Respectfully submitted,



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Date: August 31, 2009

Claims Appendix (Independent Claims 1 and 29)

1. (Previously presented) A processing system comprising a plurality of processing elements, the processing elements comprising a controller and computation means, the plurality of processing elements being dynamically reconfigurable by a cluster control signal as mutually independently operating task units that comprise one processing element or a cluster of two or more processing elements, the processing elements within a cluster being arranged to execute instructions under a common thread of program control, wherein the cluster control signal is derived from intermediate control signals transmitted through a reconfigurable channel infrastructure connected to the processing elements, wherein the reconfigurable channel infrastructure comprises a control chain with combination elements for each processing element and a switch between each pair of neighboring processing elements for locally controllably inhibiting transmission of intermediate control signals to a preceding or a succeeding processing element.

29. (Previously presented) Method for operating a processing system comprising a plurality of processing elements, the processing elements comprising a controller and computation means, the method comprising the steps of:

combining an intermediate control signal with an operation control signal of a processing element and selectively passing the combined signal to a further processing element,

deriving a cluster control signal from an operation control signal and two or more intermediate control signals, and

dynamically reconfiguring a processing element by the cluster control signal thereby dynamically reconfiguring the plurality of processing elements as mutually independently operating task units that comprise one processing element or a cluster of two or more processing elements, wherein the processing elements within a cluster execute instructions under a common thread of program control.